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ART UNIT	**PAPER NUMBER**
2687	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/650,887	DONOVAN ET AL.	
	Examiner	Art Unit	
	Marivelisse Santiago-Cordero	2687	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-258* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-17,19-47,49-77 and 79-258* is/are rejected.

7)☒ Claim(s) *18,48 and 78* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on *28 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference character(s) not mentioned in the description: "170" (Fig. 7). Corrected drawing sheets in compliance with 37 CFR 1.121(d), or amendment to the specification to add the reference character(s) in the description in compliance with 37 CFR 1.121(b) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing-sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the examiner does not accept the changes, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

2. The disclosure is objected to because of the following informalities: the term "step 134" (paragraph [0050]) should be replaced with --step 170--.

Appropriate correction is required.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

4. Claims 1, 2, 4, 6-15, 16, 31-32, 34, 36-45 are provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 11-15 and 20 of copending Application No. 10/665,252. Although the conflicting claims are not identical, they are not patentably distinct from each other because the instant application claims include all of the features of the application publication claims, except for deletion of limitations. The instant "application claims are generic/broader to species of invention covered by the application publication claims, and since without terminal disclaimer, extant species claims preclude issuance of generic application claims" (See *In re Goodman*, 29 USPQ2d 2010) and deletion of the additional limitations in the instant application claims would have been obvious to one of ordinary skill in the art.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

5. Claim 99 is objected to because of the following informalities: the limitations "a second PLL" should be corrected since there is no "first PLL" claimed before (note the dependency of the claim 99 is on claim 91). For purposes of applying prior art, the Examiner uses the dependency of claim 99 to be of claim 98, which incorporates the "first PLL". Appropriate correction is required.

6. Claims 110, 119, 150, 162, 173, 182, 213, 223, 230, 236, and 256 are objected to for the same reasons stated above for claim 99. Appropriate correction is required.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

8. Claims 94, 108, 117, 125, 138, 148, 157, 171, 180, 188, 201, 211, 219 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The limitation "said second oscillator includes a semiconductor oscillator" was not described in the specification. The specification does enable crystal oscillators, however, the limitation "said second oscillator includes a semiconductor oscillator" fails to comply with the enablement requirement; therefore, without those additional details, one of ordinary skill in the art would have been burdened by undue experimentation to make or use the claimed invention.

9. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

10. Claims 80-81 and 85 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 80 recites the limitation "said MAC device" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 81 recites the limitation "said MAC device" in line 1 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim 85 recites the limitation "said MAC device" in line 3 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

12. Claims 31, 39, 114, 120, 123, 126-128, 131, 134-135, 137, 139, 142, 145, 151, 177, 183, 186, 189-191, 194, 197-198, 200, 202, 205, 208, 214, 233, 239-241, 246-248, and 253 are rejected under 35 U.S.C. 102(e) as being anticipated by Aoyama (Patent No.: 6,763,471).

Regarding claim 31, Aoyama discloses a wireless Ethernet network device with active and low power modes, comprising; first regulating means for regulating supply voltage during the active mode and that is powered down during the low power mode (Fig. 3, reference Vdd; from col. 7, line 39 through col. 8, line 2); second regulating means, which dissipates less power than said first regulating means (Fig. 3, reference numeral 1; from col. 7, line 39 through col. 8, line 2), for regulating supply voltage during the low power mode (Fig. 3, reference numeral 1;

from col. 7, line 39 through col. 8, line 2); selecting means for selecting said first regulating means during the active mode and said second regulating means during the low power mode (from col. 7, line 39 through col. 8, line 2).

Regarding claim 39, Aoyama discloses the device of claim 31, wherein when said selecting means initiates the low power mode, said first regulating means is shut down (from col. 7, line 39 through col. 8, line 2).

Regarding claim 114, Aoyama discloses a wireless device with active and low power modes, comprising: a first oscillator that generates a first reference frequency (Fig. 3, reference numeral 3); a second oscillator that generates a second reference frequency that is lower than said first frequency (Fig. 3, reference numeral 4; col. 5, lines 9-11); a first voltage supply that supplies a first voltage level to said first oscillator (Fig. 3, reference Vdd); a second voltage supply that supplies a second voltage level that is less than said first voltage level to said second oscillator (Fig. 3, reference numeral 1); and a shutdown module that shuts down said first oscillator in said low power mode (col. 7, lines 51-52 and 59-62) and transitions from said first voltage level to said second voltage level when transitioning from said active mode to said low power mode (from col. 7, line 66 through col. 8, line 2), and that operates said first oscillator in said active mode (col. 7, lines 39-42) and transitions from said second voltage level to said first voltage level when transitioning from said low power mode to said active mode (col. 7, lines 39-49 and col. 8, lines 28-39).

Regarding claim 120, Aoyama discloses the wireless device of claim 114 (see above), wherein said first voltage supply includes a first voltage regulator and said voltage supply includes a second voltage regulator (Figs. 3 and 9).

Regarding claim 177, the limitations are rejected as stated above for claim 114.

Regarding claim 183, the limitations are rejected as stated above for claim 120.

Regarding claim 123, Aoyama discloses a wireless device with active and low power modes, comprising: a first oscillator that generates a first reference frequency (Fig. 3, reference numeral 3); a second oscillator that generates a second reference frequency that is lower than said first frequency (Fig. 3, reference numeral 4; col. 5, lines 9-11); a first wireless circuit that communicates with said first oscillator (Figs. 3 and 9); a second wireless circuit that communicates with said second oscillator (Figs. 3 and 9); and a shutdown module that shuts down said first wireless circuit and said first oscillator (col. 11, lines 12-15 and 19-26) and operates said second oscillator and said second wireless circuit during said low power mode (col. 11, lines 5-10 and 27-29), and that operates said first oscillator and said first wireless circuit during said active mode (col. 10, lines 47-63).

Regarding claim 126, Aoyama discloses the wireless device of claim 123 (see above), further comprising: a voltage supply that supplies a first voltage level to said first oscillator (Fig. 3, reference numeral 3) and a second voltage level that is less than said first voltage level to said second oscillator (Fig. 3, reference numeral 4; col. 5, lines 9-11).

Regarding claim 127, Aoyama discloses the wireless device of claim 126 (see above), wherein said voltage supply includes a first voltage supply that supplies said first voltage level to said first wireless circuit (col. 10, lines 59-63), and said second voltage supply that supplies said second voltage level to said second wireless circuit (col. 11, lines 11-29).

Regarding claim 128, Aoyama discloses the wireless device of claim 127 (see above), wherein said shutdown module transitions from said first voltage level to said second voltage

level when transitioning from said active mode to said low power mode (from col. 7, line 66 through col. 8, line 2) and transitions from said second voltage level to said first voltage level when transitioning form said low power mode to said active mode (col. 7, lines 39-49 and col. 8, lines 28-39).

Regarding claim 131, Aoyama discloses the wireless device of claim 126 (see above), wherein said first voltage supply includes a first voltage regulator and said voltage supply includes a second voltage regulator (Figs. 3 and 9).

Regarding claim 134, Aoyama discloses a wireless device with active and low power modes, comprising; a voltage supply that supplies a first voltage level and a second voltage level that is less than said first voltage level (Fig. 3, reference numerals Vdd and 1); a first wireless circuit (Figs. 3 and 9); a second wireless circuit (Figs. 3 and 9); and a shutdown module that shuts down said first wireless circuit (col. 11, lines 12-15 and 19-26) and operates said second wireless circuit in said low power mode (col. 11, lines 5-10 and 27-29) and transitions from said first voltage level to said second voltage level when transitioning from said active mode to said low power mode (from col. 7, line 66 through col. 8, line 2), and that operates said first wireless circuit in said active mode (col. 10, lines 47-63) and transitions from said second voltage level to said first voltage level when transitioning from said low power mode to said active mode (col. 7, lines 39-49 and col. 8, lines 28-39).

Regarding claim 135, Aoyama discloses the wireless device of claim 134 (see above), wherein said first voltage supply includes a first voltage supply that supplies said first voltage level and a second voltage supply that supplies said second voltage level (Figs. 3 and 9, reference numeral Vdd and 1, respectively).

Regarding claim 137, Aoyama discloses the wireless device of claim 134 (see above), further comprising: a first oscillator that communicates with said first wireless circuit (Figs. 3 and 9, reference numeral 3), that receives said first voltage level and that generates a first reference frequency (Figs. 3 and 9, reference numeral 3); and a second oscillator that receives said second voltage level, that communicates with said second wireless circuit, that consumes less power than said first oscillator and that generates a second reference frequency (Figs. 3 and 9, reference numeral 4; col. 5, lines 9-11).

Regarding claim 139, Aoyama discloses the wireless device of claim 137 (see above), wherein said shutdown module shuts down said first oscillator and operates said second oscillator during said low power mode (col. 7, lines 51-52 and 59-62) and operates said first oscillator in said active mode (col. 7, lines 39-42).

Regarding claim 142, Aoyama discloses the wireless device of claim 135 (see above), wherein said first voltage supply includes a first voltage regulator and said voltage supply includes a second voltage regulator (Figs. 3 and 9).

Regarding claim 145, Aoyama discloses a wireless device with active and low power modes, comprising; a first oscillator that generates a first reference frequency (Fig. 3, reference 3); a second oscillator that consumes less power than said first oscillator and that generates a second reference frequency (Fig. 3, reference numeral 4; col. 5, lines 9-11); a first voltage supply that supplies a first voltage level to said first oscillator (Fig. 3, reference Vdd); a second voltage supply that supplies a second voltage level that is less than said first voltage level to said second oscillator (Fig. 3, reference numeral 1); a first wireless circuit that communicates with said first oscillator (Figs. 3 and 9); a second wireless circuit that communicates with said second oscillator

(Figs. 3 and 9); and a shutdown module that shuts down said first wireless circuit and said first oscillator in said low power mode (col. 11, lines 12-15 and 19-26), operates said second wireless circuit and said second oscillator in said low power mode (col. 11, lines 5-10 and 27-29) and transitions from said first voltage level to said second voltage level when transitioning from said active mode to said low power mode (from col. 7, line 66 through col. 8, line 2), and that operates said first wireless circuit and said first oscillator in said active mode (col. 10, lines 47-63)and transitions from said second voltage level to said first voltage level when transitioning from said low power mode to said active mode (col. 7, lines 39-49 and col. 8, lines 28-39).

Regarding claim 151, Aoyama discloses the wireless device of claim 145 (see above), wherein said first voltage supply includes a first voltage regulator and said voltage supply includes a second voltage regulator (Figs. 3 and 9).

Regarding claim 186, the limitations are rejected as stated above for claim 123.

Regarding claim 189, the limitations are rejected as stated above for claim 126.

Regarding claim 190, the limitations are rejected as stated above for claim 127.

Regarding claim 191, the limitations are rejected as stated above for claim 128.

Regarding claim 194, the limitations are rejected as stated above for claim 131.

Regarding claim 197, the limitations are rejected as stated above for claim 134.

Regarding claim 198, the limitations are rejected as stated above for claim 135.

Regarding claim 200, the limitations are rejected as stated above for claim 137.

Regarding claim 202, the limitations are rejected as stated above for claim 139.

Regarding claim 205, the limitations are rejected as stated above for claim 142.

Regarding claim 208, the limitations are rejected as stated above for claim 145.

Regarding claim 214, the limitations are rejected as stated above for claim 151.

Regarding claim 233, the limitations are rejected as stated above for claim 114.

Regarding claim 239, the limitations are rejected as stated above for claim 186.

Regarding claim 240, the limitations are rejected as stated above for claim 189.

Regarding claim 241, the limitations are rejected as stated above for claim 191.

Regarding claim 246, the limitations are rejected as stated above for claim 197.

Regarding claim 247, the limitations are rejected as stated above for claim 200.

Regarding claim 248, the limitations are rejected as stated above for claim 202.

Regarding claim 253, the limitations are rejected as stated above for claim 145.

13. Claims 26, 56, 61, 69, and 86 are rejected under 35 U.S.C. 102(b) as being anticipated by Kobayashi et al. (hereinafter "Kobayashi"; Pub. No.: US 2001/00110457).

Regarding claim 26, Kobayashi discloses a baseband processor for a wireless Ethernet network device with active and low power modes, comprising; a first voltage regulator that regulates supply voltage during the active mode and that is powered down during the low power mode (page 3, paragraph [0031]); and a second voltage regulator that dissipates less power than said first voltage regulator (page 3, paragraph [0031]), and that regulates supply voltage during the low power mode (page 3, paragraph [0031]).

Regarding claims 56, 61, and 86, the limitations are rejected as stated above for claim 26.

Regarding claim 69, Kobayashi discloses the method of claim 61, further comprising shutting down said first voltage regulator when the low power mode is initiated (page 1, paragraph [0002]).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

15. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

16. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

17. Claims 1-3, 9, 16, 21-22, 32-33, 46, and 51-52, are rejected under 35 U.S.C. 102(e) as being anticipated by Aoyama in view of Amos.

Regarding claim 1, Aoyama discloses a wireless Ethernet network device with active and low power modes, comprising; a first voltage regulator that regulates supply voltage during the

active mode and that is powered down during the low power mode (Fig. 3, reference Vdd; from col. 7, line 39 through col. 8, line 2); a second voltage regulator that dissipates less power than said first voltage regulator (Fig. 3, reference numeral 1; from col. 7, line 39 through col. 8, line 2), and that regulates supply voltage during the low power mode (Fig. 3, reference numeral 1; from col. 7, line 39 through col. 8, line 2); and a controller that selects said first voltage regulator during the active mode and said second voltage regulator during the low power mode (from col. 7, line 39 through col. 8, line 2).

Aoyama fails to disclose a medium access controller (MAC).

However, Amos discloses a wireless Ethernet network device with active and low power modes comprising a medium access controller (MAC) (col. 2, lines 62-67).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the controller of Aoyama a medium access controller (MAC) device as suggested by Amos.

One of ordinary skill in this art would have been motivated to incorporate the controller in a medium access controller (MAC) device because it is required to be responsive to the host bus interface and events from a wireless or RF interface (Amos: col. 1, lines 41-43).

Regarding claim 2, Aoyama in combination with Amos fail to disclose further comprising a baseband processor (BBP) that performs radio frequency mixing and that communicates with said MAC device.

However, the Examiner takes Official Notice that it was notoriously well known in the art at the time the invention was made to incorporate a baseband processor (BBP) that performs radio frequency mixing and that communicates with said MAC device. Therefore, it would have

been obvious to one of ordinary skill in this art at the time the invention was made to incorporate a baseband processor (BBP) that performs radio frequency mixing and that communicates with said MAC device in order to obtain an optimum frequency signal for further processing.

Regarding claim 32, the limitations are rejected for the same reasons and motivations stated above for claim 2.

Regarding claim 3, Aoyama in combination with Amos disclose the device of claim 2. Aoyama in combination with Amos fail to disclose wherein at least one of said first and second voltage regulators is located in said BBP. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to locate at least one of said first and second voltage regulators of Aoyama in combination with Amos in said BBP, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893).

Regarding claim 33, the limitations are rejected for the same reasons and motivations stated above for claim 3.

Regarding claim 9, in the obvious combination, Aoyama, wherein when said MAC device initiates the low power mode, said first voltage regulator is shut down (from col. 7, line 39 through col. 8, line 2).

Regarding claim 16, in the obvious combination, Amos discloses wherein said wireless Ethernet network device is operated in an ad hoc mode (from col. 1, line 57 through col. 2, line 4).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to operate the device of Aoyama in combination with Amos in an ad hoc mode as suggested by Amos.

One of ordinary skill in this art would have been motivated to operate the device in an ad hoc mode because if the traffic indication map beacon indicates traffic is pending for the mobile unit, the mobile unit must then stay awake until it has handled all its traffic and can then return to power save mode (Amos: from col. 1, line 57 through col. 2, line 4).

Regarding claim 46, the limitations are rejected for the same reasons and motivations stated above for claim 16.

Regarding claim 21, in the obvious combination, Amos discloses wherein said MAC device includes transmit and receive state machines and a transmit buffer and further comprising initiating said low power mode when said transmit buffer is empty and said transmit and receive state machines are idle (co. 4, lines 16-38).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate in the device of Aoyama in combination with Amos wherein said MAC device includes transmit and receive state machines and a transmit buffer and further comprising initiating said low power mode when said transmit buffer is empty and said transmit and receive state machines are idle as suggested by Amos.

One of ordinary skill in this art would have been motivated to incorporate in the device wherein said MAC device includes transmit and receive state machines and a transmit buffer and further comprising initiating said low power mode when said transmit buffer is empty and said transmit and receive state machines are idle because then there is no more traffic for the MAC

and/or all of the traffic is completed, hence, the MAC can sleep until the next beacon (Amos: col. 4, lines 16-38).

Regarding claim 51, the limitations are rejected for the same reasons and motivations stated above for claim 21.

Regarding claim 22, Aoyama in combination with Amos disclose the claimed invention except for wherein said wireless Ethernet network device dissipates less than 2mW when in said low power mode. However, it would have been obvious to one of ordinary skill in this art at the time the invention was made to dissipate less than 2mW when in said low power mode, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

Regarding claim 52, the limitations are rejected for the same reasons and motivations stated above for claim 22.

18. Claims 4-8, 12-14, 17, 19, 24-25, 34-38, 42-44, 47, 49, and 54-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama in combination with Amos and further in view of Applicant's admitted prior art.

Regarding claim 4, Aoyama in combination with Amos discloses the device of claim 2. Aoyama in combination with Amos fail to disclose further comprising a first phase locked loop (PLL) that generates a first clock signal for said BBP during the active mode.

However, Applicant's admitted prior art discloses a first phase locked loop (PLL) that generates a first clock signal for said BBP during the active mode (Background of the Invention: paragraph [0003]; note that according to Applicant's admitted prior art, the BBP may include PLL which inherently generates clock signals).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a first clock signal for said BBP during the active mode of Aoyama in combination with Amos as suggested by Applicant's admitted prior art.

One of ordinary skill in this art would have been motivated to incorporate a first clock signal for said BBP during the active mode because it would conserve power (Applicant's admitted prior art: Background of the Invention, paragraph [0003]).

Regarding claim 34, the limitations are rejected for the same reasons and motivations stated above for claim 4.

Regarding claim 5, in the obvious combination, Applicant's admitted prior art discloses wherein said first PLL is located in said BBP (Background of the Invention: paragraph [0003]).

Regarding claim 35, the limitations are rejected for the same reasons and motivations stated above for claim 5.

Regarding claim 6, in the obvious combination, Applicant's admitted prior art discloses further comprising a crystal oscillator that outputs timing signal to said first PLL during the active mode (Background of the Invention: paragraph [0003]).

Regarding claim 36, the limitations are rejected for the same reasons and motivations stated above for claim 6.

Regarding claim 7, in the obvious combination, Applicant's admitted prior art discloses further comprising: a radio frequency (RF) transceiver that transmits and receives wireless signals, that communicates with said BBP and that includes a second PLL (Background of the Invention: paragraphs [0002]-[0003]; note the plurality of phase locked loops) that receives said timing signal from said crystal oscillator during the active mode and that generates a second

clock signal for said RF transceiver (Background of the Invention: paragraph [0003]; the RF transceiver may include PLL which inherently generates clock signals).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate in the device of Aoyama in combination with Amos and Applicant's admitted prior art a radio frequency (RF) transceiver that transmits and receives wireless signals, that communicates with said BBP and that includes a second PLL that receives said timing signal from said crystal oscillator during the active mode and that generates a second clock signal for said RF transceiver as suggested by Applicant's admitted prior art.

One of ordinary skill in this art would have been motivated to incorporate in the device of Aoyama in combination with Amos and Applicant's admitted prior art a radio frequency (RF) transceiver that transmits and receives wireless signals, that communicates with said BBP and that includes a second PLL that receives said timing signal from said crystal oscillator during the active mode and that generates a second clock signal for said RF transceiver because they adjust the frequency of the input signal.

Regarding claim 37, the limitations are rejected for the same reasons and motivations stated above for claim 7.

Regarding claim 8, in the obvious combination, Amos discloses further comprising a first oscillator that generates a third clock signal during the low power mode, wherein said first oscillator dissipates less power than said crystal oscillator (col. 3, lines 4-8).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a first oscillator that generates a third clock signal during the low power mode of Aoyama in combination with Amos and Applicant's admitted prior art,

wherein said first oscillator dissipates less power than said crystal oscillator as suggested by Amos.

One of ordinary skill in this art would have been motivated to incorporate a first oscillator that generates a third clock signal during the low power mode of Aoyama in combination with Amos and Applicant's admitted prior art, wherein said first oscillator dissipates less power than said crystal oscillator because it will minimize power consumption by operating the controller at the lowest clock speed necessary and by turning off the high frequency oscillator when not in use (Amos: col. 6, lines 8-11).

Regarding claim 38, the limitations are rejected for the same reasons and motivations stated above for claim 8.

Regarding claim 12, in the obvious combination, Amos discloses wherein when said MAC device initiates the low power mode, said crystal oscillator is shut down (col. 3, lines 4-8).

Regarding claim 42, the limitations are rejected for the same reasons and motivations stated above for claim 12.

Regarding claim 13, Aoyama in combination with Amos and Applicant's admitted prior art disclose the device of claim wherein said MAC device includes a counter (Amos: col. 3, lines 4-8) and wherein said MAC device initiates the low power mode, powering said counter (Amos: col. 3, lines 4-8). In addition, Aoyama in combination with Amos and Applicant's admitted prior art disclose said first voltage regulator powers said first oscillator (Figs. 3 and 9).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to power said first oscillator of Aoyama in combination with Amos and

Applicant's admitted prior art using said first voltage regulator as suggested by Aoyama because it would provide the necessary voltage (Aoyama: col. 10, lines 59-63).

Regarding claim 43, the limitations are rejected for the same reasons and motivations stated above for claim 13.

Regarding claim 14, in the obvious combination, Amos discloses wherein when said counter reaches a predetermined count, said MAC device powers up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver, said first PLL, said BB processor and said second PLL (col. 3, lines 19-25; from col. 4, line 60 through col. 5, line 3).

Regarding claim 44, the limitations are rejected for the same reasons and motivations stated above for claim 14.

Regarding claim 17, in the obvious combination, Amos discloses wherein said MAC device includes an external interface and wherein when said MAC device receives a wake up signal from a host via said external interface (col. 5, lines 7-8), said MAC device powers up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver and said first and second PLL (from col. 4, line 59 through col. 5, line 55).

Regarding claim 47, the limitations are rejected for the same reasons and motivations stated above for claim 17.

Regarding claim 19, in the obvious combination, Applicant's admitted prior art discloses wherein said crystal oscillator is an external crystal oscillator (XOSC) (Background of the Invention: paragraph [0003]).

Regarding claim 49, the limitations are rejected for the same reasons and motivations stated above for claim 19.

Regarding claim 24, the obvious combination of Aoyama, Amos and Applicant's admitted prior art fails to disclose wherein said first oscillator is located in said BB processor. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to locate first oscillator of Aoyama in said BB processor, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893).

Regarding claim 54, the limitations are rejected for the same reasons and motivations stated above for claim 24.

Regarding claim 25, the obvious combination, Applicant's admitted prior art discloses wherein at least two of said BB processor, said first voltage regulator, said second voltage regulator, said RF transceiver, said MAC device, and said first PLL are implemented using a system on chip (SOC) (Background of the Invention: paragraphs [0002]-[0003]).

Regarding claim 55, the limitations are rejected for the same reasons and motivations stated above for claim 25.

19. Claims 10-11, 40-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama in combination with Amos and Applicant's admitted prior art as applied to claim 7 above, and further in view of Guerlin.

Regarding claim 10, Aoyama in combination with Amos and Applicant's admitted prior art disclose the device of claim 7. Aoyama in combination with Amos and Applicant's admitted prior art fail to disclose wherein when said MAC device initiates the low power mode said RF transceiver is shut down.

However, Guerlin discloses wherein when said MAC device initiates the low power mode said RF transceiver is shut down (col. 2, lines 33-39).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant incorporate wherein when said MAC device of Aoyama in combination with Amos and Applicant's admitted prior art initiates the low power mode, shutting down the RF transceiver as suggested by Guerlin.

One of ordinary skill in this art would have been motivated to shut down the RF transceiver when the MAC device initiates the low power mode in order to maximize energy conservation (Guerlin: col. 2, lines 33-39).

Regarding claim 40, the limitations are rejected for the same reasons and motivations stated above for claim 10.

Regarding claim 11, Aoyama in combination with Amos and Applicant's admitted prior art disclose the method of claim 7. Aoyama in combination with Amos and Applicant's admitted prior art fail to wherein when said MAC device initiates the low power mode, said first and second PLL are shut down (note, however, that Applicant's admitted prior art discloses the first and second PLL may be included in the RF transceiver).

However, Guerlin discloses shutting down said first and second PLL when said MAC device initiates the low power mode (col. 2, lines 33-39; note that Guerlin shuts down the circuits in the transceiver).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to shut down said first and second PLL of Aoyama in combination with

Amos and Applicant's admitted prior art when said MAC device initiates the low power mode as suggested by Guerlin.

One of ordinary skill in this art would have been motivated to shut down said first and second PLL when said MAC device initiates the low power mode in order to maximize energy conservation (Guerlin: col. 2, lines 33-39).

Regarding claim 41, the limitations are rejected for the same reasons and motivations stated above for claim 11.

20. Claims 15 and 45 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama in combination with Amos as applied to claim 1 above, and further in view of Applicant's admitted prior art.

Regarding claim 15, Aoyama in combination with Amos discloses the wireless Ethernet network device of claim 1. Aoyama in combination with Amos fail to disclose wherein said wireless Ethernet network device is operated in an infrastructure mode.

However, Applicant's admitted prior art discloses wherein said wireless Ethernet network device is operated in an infrastructure mode (Background of the Invention: paragraph [0004]).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to operate the device of Aoyama in combination with Amos in an infrastructure mode as suggested by Applicant's admitted prior art.

One of ordinary skill in this art would have been motivated to operate the device in an infrastructure mode because the host communicates with a network via the Ethernet network device and an access point (Background of the Invention: paragraph [0004]).

Regarding claim 45, the limitations are rejected for the same reasons and motivations stated above for claim 15.

21. Claims 20 and 50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama in combination with Amos and Applicant's admitted prior art as applied to claim 6 above, and further in view of Pohjonen (Patent No.: 6,944,432).

Regarding claim 20, Aoyama in combination with Amos and Applicant's admitted prior art disclose the device of claim 6 wherein said crystal oscillator includes an external crystal (Background of the Invention: paragraph [0003]). Aoyama in combination with Amos and Applicant's admitted prior art fails to disclose wherein said crystal oscillator includes an amplifier that is integrated with one of said MAC device, said BB processor, and said RF transceiver.

However, Pohjonen discloses a method for a wireless network device wherein said crystal oscillator includes an external crystal and an amplifier that is integrated with one of said MAC device, said BB processor, and said RF transceiver (col. 1, lines 56-59; note that the PLLs may be included in the BB processor and/or the RF transceiver as suggested by Applicant's admitted prior art).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include in the crystal oscillator of Aoyama in combination with Amos and Applicant's admitted prior art an external crystal and an amplifier that integrates with one of said MAC device, said BB processor, and said RF transceiver as suggested by Pohjonen.

One of ordinary skill in this art would have been motivated to include in the crystal oscillator an external crystal and an amplifier that integrates with one of said MAC device, said

BB processor, and said RF transceiver because it would further integrate the components (Pohjonen: col. 1, lines 56-59).

Regarding claim 50, the limitations are rejected for the same reasons and motivations stated above for claim 20.

22. Claims 23 and 53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama in combination with Amos and Applicant's admitted prior art as applied to claim 6 above, and further in view of Chapman.

Regarding claim 23, Aoyama in combination with Amos and Applicant's admitted prior art disclose the device of claim 6, further comprising a processor that communicates with said crystal oscillator (Aoyama: Figs. 3 and 6). Aoyama in combination with Amos and Applicant's admitted prior art fail to disclose further comprising a processor that calibrates said first oscillator using said timing signal from said crystal oscillator.

However, Chapman discloses further comprising a processor that calibrates said first oscillator using said timing signal from said crystal oscillator (from col. 2, line 65 through col. 3, line 5).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to calibrate said first oscillator using said timing signal from said crystal oscillator of Aoyama in combination with Amos and Applicant's admitted prior art as suggested by Chapman.

One of ordinary skill in this art would have been motivated to calibrate said first oscillator using said timing signal from said crystal oscillator because it would compensate for

the inaccuracy of the oscillator due to its dependence upon voltage, process and temperature and it's inherent frequency instability (Chapman: from col. 2, line 65 through col. 3, line 5).

Regarding claim 53, the limitations are rejected for the same reasons and motivations stated above for claim 23.

23. Claims 27, 57, 81, and 87 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Amos (Patent No.: 6,934,870).

Regarding claim 27, Kobayashi discloses the processor of claim 26 (see above). Kobayashi fails to disclose wherein said baseband processor receives a power mode select signal from a medium access controller.

However, Amos discloses a processor for a wireless Ethernet network device with active and low power modes wherein said baseband processor receives a power mode select signal from a medium access controller (col. 3, lines 3-8).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to receive a power mode select signal of Kobayashi from a medium access controller as suggested by Amos.

One of ordinary skill in this art would have been motivated to receive a power mode select signal from a medium access controller because the MAC is required to be response to the components and events from the wireless or RF interface (Amos: col. 1, lines 42-43).

Regarding claims 57 and 87, the limitations are rejected for the same reasons and motivations stated above for claim 27.

Regarding claim 81, Kobayashi discloses the processor of claim 61 (see above). Kobayashi fails to disclose wherein said MAC device includes transmit and receive state

machines and a transmit buffer and further comprising initiating said low power mode when said transmit buffer is empty and said transmit and receive state machines are idle.

However, Amos discloses a method for operating a wireless Ethernet network device with active and low power modes wherein said MAC device includes transmit and receive state machines and a transmit buffer and further comprising initiating said low power mode when said transmit buffer is empty and said transmit and receive state machines are idle (co. 4, lines 16-38).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate in the method of Kobayashi wherein said MAC device includes transmit and receive state machines and a transmit buffer and further comprising initiating said low power mode when said transmit buffer is empty and said transmit and receive state machines are idle as suggested by Amos.

One of ordinary skill in this art would have been motivated to incorporate in the method wherein said MAC device includes transmit and receive state machines and a transmit buffer and further comprising initiating said low power mode when said transmit buffer is empty and said transmit and receive state machines are idle because then there is no more traffic for the MAC and/or all of the traffic is completed, hence, the MAC can sleep until the next beacon (Amos: col. 4, lines 16-38).

24. Claims 62-63 and 82 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi.

Regarding claim 62, Kobayashi discloses the method of claim 61. Kobayashi fails to disclose further comprising performing radio frequency mixing using a baseband (BB) processor.

However, the Examiner takes Official Notice that it was notoriously well known in the art at the time the invention was made to perform radio frequency mixing using a baseband (BB) processor. Therefore, it would have been obvious to one of ordinary skill in this art at the time the invention was made to perform radio frequency mixing using a baseband (BB) processor in order to obtain an optimum frequency signal for further processing.

Regarding claim 63, Kobayashi discloses the method of claim 62. Kobayashi fails to disclose further comprising locating at least on of said first and second voltage regulators in said BB processor. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to locate at least one of said first and second voltage regulators of Kobayashi in said BB processor, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893).

Regarding claim 82, Kobayashi discloses the claimed invention except for wherein said wireless Ethernet network device dissipates less than 2mW when in said low power mode. However, it would have been obvious to one of ordinary skill in this art at the time the invention was made to dissipate less than 2mW when in said low power mode, since it has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

25. Claims 28-29, 58-59, 64-67, 75, 79, and 88-89 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Applicant's admitted prior art.

Regarding claim 28, Kobayashi discloses the processor of claim 26. Kobayashi fails to disclose further comprising a first phase locked loop (PLL) that generates a first clock signal for said BBP during the active mode and that is powered down during the low power mode.

However, Applicant's admitted prior art discloses a first phase locked loop (PLL) that generates a first clock signal for said BBP during the active mode and that is powered down during the low power mode (Background of the Invention: paragraph [0003]; note that according to Applicant's admitted prior art, the BBP may include PLL which inherently generates clock signals, and the MAC device instructs the BBP to transition to a low power mode).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate a first clock signal for said BBP during the active mode of Kobayashi and that is powered down during the low power mode as suggested by Applicant's admitted prior art.

One of ordinary skill in this art would have been motivated to incorporate a first clock signal for said BBP during the active mode and that is powered down during the low power mode because it would conserve power (Applicant's admitted prior art: Background of the Invention, paragraph [0003]).

Regarding claim 29, in the obvious combination, Applicant's admitted prior art discloses wherein said first PLL receives a timing signal from a crystal oscillator during the active mode (Background of the Invention: paragraph [0003]).

Regarding claims 58 and 88, the limitations are rejected for the same reasons and motivations stated above for claim 28.

Regarding claims 59 and 89, the limitations are rejected for the same reasons and motivations stated above for claim 29.

Regarding claim 64, Kobayashi discloses the method of claim 62. Kobayashi fails to disclose further comprising generating a first clock signal for said BB processor during the active mode using a first phase locked loop (PLL).

However, Applicant's admitted prior art discloses generating a first clock signal for said BB processor during the active mode using a first phase locked loop (PLL) (Background of the Invention: paragraph [0003]; note that according to Applicant's admitted prior art, the BBP may include PLL which inherently generates clock signals, and the MAC device instructs the BBP to transition to a low power mode).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to generate a first clock signal for said BB processor during the active mode of Kobayashi using a first phase locked loop as suggested by Applicant's admitted prior art.

One of ordinary skill in this art would have been motivated to generate a first clock signal for said BB processor during the active mode using a first phase locked loop because it would conserve power (Applicant's admitted prior art: Background of the Invention, paragraph [0003]).

Regarding claim 65, in the obvious combination, Applicant's admitted prior art discloses wherein said first PLL is located in said BB processor (Background of the Invention: paragraph [0003]).

Regarding claim 66, in the obvious combination, Applicant's admitted prior art discloses further comprising generating a timing signal for said first PLL using a crystal oscillator during the active mode (Background of the Invention: paragraph [0003]).

Regarding claim 67, in the obvious combination, Applicant's admitted prior art discloses further comprising: transmitting and receiving wireless signals using a radio frequency (RF) transceiver that includes a second PLL (Background of the Invention: paragraphs [0002]-[0003]; note the plurality of phase locked loops); and receiving said timing signal from said crystal oscillator at said second PLL during the active mode and generating a second clock signal for said RF transceiver (Background of the Invention: paragraph [0003]; the RF transceiver may include PLL which inherently generates clock signals).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate in the method of Kobayashi transmitting and receiving wireless signals using a radio frequency (RF) transceiver that includes a second PLL; and receiving said timing signal from said crystal oscillator at said second PLL during the active mode and generating a second clock signal for said RF transceiver as suggested by Applicant's admitted prior art.

One of ordinary skill in this art would have been motivated to incorporate in the method transmitting and receiving wireless signals using a radio frequency (RF) transceiver that includes a second PLL; and receiving said timing signal from said crystal oscillator at said second PLL during the active mode and generating a second clock signal for said RF transceiver because they adjust the frequency of the input signal.

Regarding claim 75, Kobayashi discloses the method of claim 61. Kobayashi fails to disclose wherein said wireless Ethernet network device is operated in an infrastructure mode.

However, Applicant's admitted prior art discloses wherein said wireless Ethernet network device is operated in an infrastructure mode (Background of the Invention: paragraph [0004]).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to operate the device of Kobayashi in an infrastructure mode as suggested by Applicant's admitted prior art.

One of ordinary skill in this art would have been motivated to operate the device in an infrastructure mode because the host communicates with a network via the Ethernet network device and an access point (Background of the Invention: paragraph [0004]).

Regarding claim 79, in the obvious combination, Applicant's admitted prior art discloses wherein said crystal oscillator is an external crystal oscillator (XOSC) (Background of the Invention: paragraph [0003]).

26. Claim 80 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in combination with Applicant's admitted prior art as applied to claim 66 above, and further in view of Pohjonen (Patent No.: 6,944,432).

Regarding claim 80, Kobayashi in combination with Applicant's admitted prior art disclose the method of claim 66 wherein said crystal oscillator includes an external crystal (Background of the Invention: paragraph [0003]). Kobayashi in combination with Applicant's admitted prior art fails to disclose wherein said crystal oscillator includes an amplifier and further comprising integrating said amplifier with one of said MAC device, said BB processor, and said RF transceiver.

However, Pohjonen discloses a method for a wireless network device wherein said crystal oscillator includes an external crystal and an amplifier and further comprising integrating said amplifier with one of said MAC device, said BB processor, and said RF transceiver (col. 1, lines 56-59; note that the PLLs may be included in the BB processor and/or the RF transceiver as suggested by Applicant's admitted prior art).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include in the crystal oscillator of Kobayashi in combination with Applicant's admitted prior art an external crystal and an amplifier and further comprising integrating said amplifier with one of said MAC device, said BB processor, and said RF transceiver as suggested by Pohjonen.

One of ordinary skill in this art would have been motivated to include in the crystal oscillator an external crystal and an amplifier and further comprising integrating said amplifier with one of said MAC device, said BB processor, and said RF transceiver because it would further integrate the components (Pohjonen: col. 1, lines 56-59).

27. Claims 30, 60, 68, 72, 77, 84-85, and 90 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in combination with Applicant's admitted prior art, and further in view of Amos.

Regarding claim 30, Kobayashi in combination with Applicant's admitted prior art discloses the processor of claim 29. Kobayashi in combination with Applicant's admitted prior art fail to disclose further comprising a first oscillator that generates a second clock signal during the low power mode, wherein said first oscillator dissipates less power than the crystal oscillator.

However, Amos discloses a processor for a wireless Ethernet network device with active and low power modes further comprising a first oscillator that generates a second clock signal during the low power mode, wherein said first oscillator dissipates less power than the crystal oscillator (col. 3, lines 4-8).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate in the processor of Kobayashi in combination with Applicant's admitted prior art a first oscillator that generates a second clock signal during the low power mode, wherein said first oscillator dissipates less power than the crystal oscillator as suggested by Amos.

One of ordinary skill in this art would have been motivated to incorporate in the processor a first oscillator that generates a second clock signal during the low power mode, wherein said first oscillator dissipates less power than the crystal oscillator because it will minimize power consumption by operating the controller at the lowest clock speed necessary and by turning off the high frequency oscillator when not in use (Amos: col. 6, lines 8-11).

Regarding claims 60 and 90, the limitations are rejected for the same reasons and motivations stated above for claim 30.

Regarding claim 68, Kobayashi in combination with Applicant's admitted prior art discloses the method of claim 67. Kobayashi in combination with Applicant's admitted prior art fail to disclose further comprising generating a third clock signal during the low power mode using a first oscillator, wherein said first oscillator dissipates less power than said crystal oscillator.

However, Amos discloses a method for operating a wireless Ethernet network device with active and low power modes further comprising generating a third clock signal during the low power mode using a first oscillator, wherein said first oscillator dissipates less power than said crystal oscillator (col. 3, lines 4-8).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to generate a third clock signal during the low power mode of Kobayashi in combination with Applicant's admitted prior art using a first oscillator, wherein said first oscillator dissipates less power than said crystal oscillator as suggested by Amos.

One of ordinary skill in this art would have been motivated to generate a third clock signal during the low power mode using a first oscillator, wherein said first oscillator dissipates less power than said crystal oscillator because it will minimize power consumption by operating the controller at the lowest clock speed necessary and by turning off the high frequency oscillator when not in use (Amos: col. 6, lines 8-11).

Regarding claim 72, Kobayashi in combination with Applicant's admitted prior art discloses the method of claim 67. Kobayashi in combination with Applicant's admitted prior art fail to disclose further comprising shutting down said crystal oscillator when the low power mode is initiated.

However, Amos discloses a method for operating a wireless Ethernet network device with active and low power modes further comprising shutting down said crystal oscillator when the low power mode is initiated (col. 3, lines 4-8).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to shut down the crystal oscillator of Kobayashi in combination with Applicant's admitted prior art when the low power mode is initiated as suggested by Amos.

One of ordinary skill in this art would have been motivated to shut down the crystal oscillator when the low power mode is initiated because it would minimize power consumption (Amos: col. 6, lines 8-11).

Regarding claim 77, Kobayashi in combination with Applicant's admitted prior art discloses the method of claim 67. Kobayashi in combination with Applicant's admitted prior art fail to disclose further comprising powering up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver, said first PLL, and second PLL when a wake up signal from a host is received.

However, Amos discloses a method for operating a wireless Ethernet network device with active and low power modes further comprising powering up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver, said first PLL, and second PLL when a wake up signal from a host is received (col. 5, lines 20-55).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to power up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver, said first PLL, and second PLL of Kobayashi in combination with Applicant's admitted prior art when a wake up signal from a host is received as suggested by Amos.

One of ordinary skill in this art would have been motivated to power up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver, said first PLL, and second

PLL when a wake up signal from a host is received because it would enable the device to determine if the traffic received requires activity for the RF or wireless interface (Amos: col. 5, lines 20-55).

Regarding claim 84, the obvious combination of Kobayashi, Applicant's admitted prior art, and Amos fails to disclose further comprising locating said first oscillator in said BB processor. However, it would have been obvious to one having ordinary skill in the art at the time the invention was made to locate first oscillator of Kobayashi in said BB processor, since it has been held that forming in one piece an article which has formerly been formed in two pieces and put together involves only routine skill in the art. *Howard v. Detroit Stove Works*, 150 U.S. 164 (1893).

Regarding claim 85, the obvious combination, Applicant's admitted prior art discloses further comprising implementing at least two of said BB processor, said first voltage regulator, said second voltage regulator, said RF transceiver, said MAC device, and said first PLL using a system on chip (SOC) (Background of the Invention: paragraphs [0002]-[0003]).

28. Claims 70-71 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in combination with Applicant's admitted prior art as applied to claim 67 above, and further in view of Guerlin.

Regarding claim 70, Kobayashi in combination with Applicant's admitted prior art disclose the method of claim 67. Kobayashi in combination with Applicant's admitted prior art fail to disclose further comprising shutting down said RF transceiver when the low power mode is initiated.

However, Guerlin discloses shutting down said RF transceiver when the low power mode is initiated (col. 2, lines 33-39).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to shut down the RF transceiver of Kobayashi in combination with Applicant's admitted prior art when the low power mode is initiated as suggested by Guerlin.

One of ordinary skill in this art would have been motivated to shut down the RF transceiver when the low power mode is initiated because in order to maximize energy conservation (Guerlin: col. 2, lines 33-39).

Regarding claim 71, Kobayashi in combination with Applicant's admitted prior art disclose the method of claim 67. Kobayashi in combination with Applicant's admitted prior art fail to disclose further comprising shutting down said first and second PLL when the low power mode is initiated (note, however, that Applicant's admitted prior art discloses the first and second PLL may be included in the RF transceiver).

However, Guerlin discloses shutting down said first and second PLL when the low power mode is initiated (col. 2, lines 33-39; note that Guerlin shuts down the circuits in the transceiver).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to shut down said first and second PLL of Kobayashi in combination with Applicant's admitted prior art when the low power mode is initiated as suggested by Guerlin.

One of ordinary skill in this art would have been motivated to shut down said first and second PLL when the low power mode is initiated because in order to maximize energy conservation (Guerlin: col. 2, lines 33-39).

29. Claims 73-74 rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in combination with Applicant's admitted prior art and Amos as applied to claim 68 above, and further in view of Aoyama.

Regarding claim 73, Kobayashi in combination with Applicant's admitted prior art and Amos disclose the method of claim 68 further comprising starting a counter when the low power mode is initiated (Amos: col. 3, lines 4-8). Kobayashi in combination with Applicant's admitted prior art and Amos fail to disclose powering said first oscillator using said first voltage regulator.

However, Aoyama discloses powering said first oscillator using said first voltage regulator (Figs. 3 and 9).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to power said first oscillator of Applicant's admitted prior art and Amos using said first voltage regulator as suggested by Aoyama.

One of ordinary skill in this art would have been motivated to power said first oscillator using said first voltage regulator because it would provide the necessary voltage (Aoyama: col. 10, lines 59-63).

Regarding claim 74, in the obvious combination, Amos discloses further comprising powering up at least two of said crystal oscillator, said first voltage regulator, said RF transceiver, said first PLL, said BB processor and said second PLL when said counter reaches a predetermined count (col. 3, lines 19-25; from col. 4, line 60 through col. 5, line 3).

30. Claim 76 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in view of Amos.

Regarding claim 76, Kobayashi discloses the method of claim 61. Kobayashi fails to disclose wherein said wireless Ethernet network device is operated in an ad hoc mode.

However, Amos discloses a method for operating a wireless Ethernet network device with active and low power modes wherein said wireless Ethernet network device is operated in an ad hoc mode (from col. 1, line 57 through col. 2, line 4).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to operate the device of Kobayashi in an ad hoc mode as suggested by Amos.

One of ordinary skill in this art would have been motivated to operate the device in an ad hoc mode because if the traffic indication map beacon indicates traffic is pending for the mobile unit, the mobile unit must then stay awake until it has handled all its traffic and can then return to power save mode (Amos: from col. 1, line 57 through col. 2, line 4).

31. Claim 83 is rejected under 35 U.S.C. 103(a) as being unpatentable over Kobayashi in combination with Applicant's admitted prior art as applied to claim 66 above, and further in view of Chapman.

Regarding claim 83, Kobayashi in combination with Applicant's admitted prior art disclose the method of claim 66. Kobayashi in combination with Applicant's admitted prior art fail to disclose further comprising calibrating said first oscillator using said timing signal from said crystal oscillator.

However, Chapman discloses further comprising calibrating said first oscillator using said timing signal from said crystal oscillator (from col. 2, line 65 through col. 3, line 5).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to calibrate said said first oscillator using said timing signal from said crystal oscillator of Kobayashi in combination with Applicant's admitted prior art as suggested by Chapman.

One of ordinary skill in this art would have been motivated to calibrate said first oscillator using said timing signal from said crystal oscillator because it would compensate for the inaccuracy of the oscillator due to its dependence upon voltage, process and temperature and it's inherent frequency instability (Chapman: from col. 2, line 65 through col. 3, line 5).

32. Claims 116, 122, 124, 130, 133, 136, 141, 144, 147, 153, 179, 185, 187, 193, 196, 199, 204, 207, 210, 216, 238, 243, 245, 250, 252, and 258 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama in view of Amos (Patent No.: 6,934,870).

Regarding claim 116, Aoyama discloses the wireless device of claim 114 (see above). Aoyama fails to disclose further comprising a medium access controller (MAC) device that includes said shutdown module.

However, Amos discloses a wireless device with active and low power modes further comprising a medium access controller (MAC) device that includes said shutdown module (from col. 2, line 61 through col. 3, line 8).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the shutdown module of Aoyama in a medium access controller (MAC) device as suggested by Amos.

One of ordinary skill in this art would have been motivated to include the shutdown module in a medium access controller (MAC) device because it is required to be responsive to the host bus interface and events from a wireless or RF interface (Amos: col. 1, lines 41-43).

Regarding claim 122, Aoyama discloses a system comprising the wireless device of claim 114 (see above). Aoyama fails to disclose further comprising a remote device for periodically transmitting a beacon, wherein said shutdown module transitions said wireless device from said low power mode prior to receiving a beacon.

However, Amos discloses a system comprising a wireless device with active and low power modes further comprising a remote device for periodically transmitting a beacon, wherein said shutdown module transitions said wireless device from said low power mode prior to receiving a beacon (col. 1, lines 62-65; col. 5, lines 1-8).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to further comprise in the system of Aoyama remote device for periodically transmitting a beacon, wherein said shutdown module transitions said wireless device from said low power mode prior to receiving a beacon as suggested by Amos.

One of ordinary skill in this art would have been motivated to further comprise in the system remote device for periodically transmitting a beacon, wherein said shutdown module transitions said wireless device from said low power mode prior to receiving a beacon because the system would determine if there is any activity that needs to be handled (Amos: col. 5, lines 8-9).

Regarding claim 124, the limitations are rejected for the same reasons and motivations stated above for claim 116.

Regarding claim 130, the limitations are rejected for the same reasons and motivations stated above for claim 141.

Regarding claim 133, the limitations are rejected for the same reasons and motivations stated above for claim 122.

Regarding claim 136, the limitations are rejected for the reasons and motivations stated above for claim 116.

Regarding claim 141, Aoyama discloses the wireless device of claim 134 (see above). Aoyama fails to disclose wherein said first wireless circuit includes at least one of a base band processor (BBP) and/or a radio frequency (FR) transmitter.

However, Amos discloses a wireless device with active and low power modes wherein said first wireless circuit includes at least one of a base band processor (BBP) and/or a radio frequency (FR) transmitter (col. 5, lines 28-30).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include in the device of Aoyama at least one of a base band processor (BBP) and/or a radio frequency (FR) transmitter as suggested by Amos.

One of ordinary skill in this art would have been motivated to include in the device of Aoyama at least one of a base band processor (BBP) and/or a radio frequency (FR) transmitter because it would be able to receive beacons in order for the MAC to handle the activity (col. 5, lines 7-9).

Regarding claims 144, 153, 185, 196, 207, 216, 238, 245, 252, and 258, the limitations are rejected for the same reasons and motivations stated above for claim 122.

Regarding claim 147, 179, 187, 199, and 210, the limitations are rejected for the same reasons and motivations stated above for claim 116.

Regarding claim 193, 204, 243, and 250, the limitations are rejected for the same reasons and motivations stated above for claim 141.

33. Claims 115, 146, 178, 209, 234, and 254 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama in view of Guerlin et al. (hereinafter "Guerlin"; Patent No.: 5,870,680).

Regarding claim 115, Aoyama discloses the wireless device of Claim 114 (see above) wherein said shutdown module shuts down the different system components (col. 11, lines 22-25). Aoyama fails to disclose further comprising: a radio frequency (RF) transceiver that communicates with said first oscillator and that transmits and receives RF signals; and a baseband processor (BBP) that communicates with said first oscillator and said RF transceiver and that performs RF mixing, wherein said shutdown module shuts down said RF transceiver and said BBP during said low power mode and operates said BBP and said RF transceiver during said active mode.

However, Guerlin discloses a wireless device with active and low power modes comprising: a radio frequency (RF) transceiver that communicates with said first oscillator and that transmits and receives RF signals (Fig. 1, reference numeral 11; col. 1, lines 55-63); and a baseband processor (BBP) that communicates with said first oscillator and said RF transceiver and that performs RF mixing (col. 1, lines 55-63), wherein said shutdown module shuts down said RF transceiver and said BBP during said low power mode (col. 2, lines 33-39) and operates said BBP and said RF transceiver during said active mode (col. 2, lines 30-33).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate in the wireless device of Aoyama a radio frequency (RF) transceiver that communicates with said first oscillator and that transmits and receives RF signals; and a baseband processor (BBP) that communicates with said first oscillator and said RF transceiver and that performs RF mixing, wherein said shutdown module shuts down said RF transceiver and said BBP during said low power mode and operates said BBP and said RF transceiver during said active mode as suggested by Guerlin.

One of ordinary skill in this art would have been motivated to incorporate in the wireless device a radio frequency (RF) transceiver that communicates with said first oscillator and that transmits and receives RF signals; and a baseband processor (BBP) that communicates with said first oscillator and said RF transceiver and that performs RF mixing because they are all typical components in a wireless device, e.g., a mobile phone (Guerlin: col. 1, lines 55-63), wherein said shutdown module shuts down said RF transceiver and said BBP during said low power mode and operates said BBP and said RF transceiver during said active mode for maximum energy conservation (Guerlin: col. 2, lines 33-39).

Regarding claims 146, 178, 209, 234, 254 the limitations are rejected for the same reasons and motivations stated above for claim 115.

34. Claims 91-93, 102, 154-156, 165, 217-218, and 225 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amos in view of Guerlin.

Regarding claim 91, Amos discloses a wireless device with active and low power modes, comprising; an oscillator that generates a first reference frequency and a second reference frequency that is lower than said first reference frequency; radio frequency (RF) transceiver that

communicates with said oscillator and that transmits and receives RF signals (col. 1, lines 58-60; col. 5, lines 7-8, 27-30, and 53-55); and a shutdown module transitions from said first frequency to said second frequency when transitioning from said active mode to said low power mode (col. 2, lines 40-43), and transitions from said second frequency to said first frequency when transitioning from said low power mode to said active mode (col. 2, lines 50-53).

Amos fails to disclose a baseband processor (BBP) that communicates with said oscillator and said RF transceiver and that performs RF mixing; and a shutdown module that shuts down said BBP and said RF transceiver in said low power mode and that operates said BBP and said RF transceiver in said active mode.

However, Guerlin discloses a wireless device with active and low power modes comprising: a radio frequency (RF) transceiver that communicates with said first oscillator and that transmits and receives RF signals (Fig. 1, reference numeral 11; col. 1, lines 55-63); a baseband processor (BBP) that communicates with said first oscillator and said RF transceiver and that performs RF mixing (col. 1, lines 55-63), and a shutdown module shuts down said RF transceiver and said BBP during said low power mode (col. 2, lines 33-39) and operates said BBP and said RF transceiver during said active mode (col. 2, lines 30-33).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate in the wireless device of Amos a baseband processor (BBP) that communicates with said first oscillator and said RF transceiver and that performs RF mixing, wherein said shutdown module shuts down said RF transceiver and said BBP during said low power mode and operates said BBP and said RF transceiver during said active mode as suggested by Guerlin.

One of ordinary skill in this art would have been motivated to incorporate in the wireless device a radio frequency (RF) transceiver that communicates with said first oscillator and that transmits and receives RF signals; and a baseband processor (BBP) that communicates with said first oscillator and said RF transceiver and that performs RF mixing because they are all typical components in a wireless device, e.g., a mobile phone (Guerlin: col. 1, lines 55-63), wherein said shutdown module shuts down said RF transceiver and said BBP during said low power mode and operates said BBP and said RF transceiver during said active mode for maximum energy conservation (Guerlin: col. 2, lines 33-39).

Regarding claim 92, in the obvious combination, Amos discloses wherein said oscillator includes a first oscillator that generates said first reference frequency (Fig. 1, reference numeral 108) and a second oscillator that consumes less power than said first oscillator and that generates said second reference frequency (Fig. 1, reference numeral 110).

Regarding claim 93, in the obvious combination, Amos discloses further comprising a medium access control (MAC) device that includes said shutdown module (col. 3, lines 3-4).

Regarding claim 102, in the obvious combination, Amos discloses a system comprising a wireless device with active and low power modes further comprising a remote device for periodically transmitting a beacon, wherein said shutdown module transitions said wireless device from said low power mode prior to receiving a beacon (col. 1, lines 62-65; col. 5, lines 1-8).

Regarding claims 154 and 217, the limitations are rejected for the same reasons and motivations stated above for claim 91.

Regarding claims 155 and 218, the limitations are rejected for the same reasons and motivations stated above for claim 92.

Regarding claim 156, the limitations are rejected for the same reasons and motivations stated above for claim 93.

Regarding claims 165 and 225, the limitations are rejected for the same reasons and motivations stated above for claim 102.

35. Claims 94, 101, 157, 164, 219, and 224 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amos in combination with Guerlin (hereinafter "Amos/Guerlin") as applied to claim 92 above, and further in view of Chapman et al. (hereinafter "Chapman"; Patent No.: 5,845,204).

Regarding claim 94, Amos/Guerlin discloses the wireless device of claim 92 (see above) wherein said first oscillator includes a crystal oscillator (Amos: col. 4, lines 64-66). Amos/Guerlin fails to disclose said second oscillator includes a semiconductor oscillator.

However, Chapman discloses a wireless device with active and low power modes wherein said first oscillator includes a crystal oscillator (col. 4, lines 33-54) and said second oscillator includes a semiconductor oscillator (col. 4, lines 33-54).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the second oscillator of Amos/Guerlin to include a semiconductor oscillator as suggested by Chapman.

One of ordinary skill in this art would have been motivated to incorporate the second oscillator to include a semiconductor oscillator because it has the characteristics of drawing very little power in both sleep and stop modes (Chapman: col. 4, lines 39-43).

Regarding claim 101, Amos/Guerlin discloses the wireless device of claim 92 (see above). Amos/Guerlin fail to disclose wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode.

However, Chapman discloses a wireless device with active and low power modes wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode (from col. 2, line 65 through col. 3, line 5).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to calibrate said second reference frequency of said second oscillator using said first reference frequency of said first oscillator of Amos/Guerlin before transitioning to said low power mode as suggested by Chapman.

One of ordinary skill in this art would have been motivated to calibrate said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode because it would compensate for the inaccuracy of the semiconductor oscillator due to its dependence upon voltage, process and temperature and it's inherent frequency instability (Chapman: from col. 2, line 65 through col. 3, line 5).

Regarding claims 157 and 219, the limitations are rejected for the same reasons and motivations stated above for claim 94.

Regarding claims 164 and 224, the limitations are rejected for the same reasons and motivations stated above for claim 101.

36. Claims 95-97, 100, 158-160, 163, and 220-221 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amos in combination with Guerlin (hereinafter "Amos/Guerlin") as applied to claim 91 above, and further in view of Aoyama.

Regarding claim 95, Amos/Guerlin disclose the wireless device of claim 91 (see above). Amos/Guerlin fails to disclose further comprising a voltage supply that supplies a first voltage level during said active mode and a second voltage level during said low power mode.

However, Aoyama discloses a voltage supply that supplies a first voltage level during said active mode and a second voltage level during said low power mode (Figs. 3 and 9; from col. 7 line 51 through col. 8, line 2).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate in the wireless device of Amos/Guerlin a voltage supply that supplies a first voltage level during said active mode and a second voltage level during said low power mode as suggested by Aoyama.

One of ordinary skill in this art would have been motivated to incorporate in the wireless device a voltage supply that supplies a first voltage level during said active mode and a second voltage level during said low power mode because it is capable of reducing power consumption (Aoyama: col. 1, lines 12-14).

Regarding claim 96, in the obvious combination, Aoyama discloses wherein said voltage supply includes a first voltage supply that supplies said first voltage level (Figs. 3 and 9; reference Vdd) and a second voltage supply that supplies said second voltage level (Figs. 3 and 9; reference 1; from col. 7, line 66 through col. 8, line 2).

Regarding claim 97, in the obvious combination, Aoyama discloses wherein said shutdown module transitions from said first voltage level to said second voltage level when transitioning from said active mode to said low power mode (from col. 7, line 66 through col. 8, line 2) and transitions from said second voltage level to said first voltage level when transitioning from said low power mode to said active mode (col. 7, lines 39-49 and col. 8, lines 28-39).

Regarding claim 100, in the obvious combination, Aoyama discloses wherein said first voltage supply includes a first voltage regulator and said second voltage supply includes a second voltage regulator (Figs. 3 and 9).

Regarding claim 158 and 220, the limitations are rejected for the same reasons and motivations stated above for claim 95.

Regarding claims 159, the limitations are rejected for the same reasons and motivations stated above for claim 96.

Regarding claims 160 and 221 the limitations are rejected for the same reasons and motivations stated above for claim 97.

Regarding claim 163, the limitations are rejected for the same reasons and motivations stated above for claim 100.

37. Claims 98-99, 161-162, and 222-223 are rejected under 35 U.S.C. 103(a) as being unpatentable over Amos/Guerlin as applied to claim 91 above, and further in view of Applicant's admitted prior art.

Regarding claim 98, Amos/Guerlin disclose the wireless device of claim 91 (see above), wherein the shutdown module shuts down the circuits of the transceiver during said low power

mode (Guerlin: col. 2, lines 33-39) and operates the circuits of the transceiver during said active move (Guerlin: col. 2, lines 30-39). Amos/Guerlin fail to disclose wherein said RF transceiver includes a first phase locked loop (PLL).

However, Applicant's admitted prior art discloses wherein said RF transceiver includes a first phase locked loop (PLL) (Background of the Invention: paragraph [0003]).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include in the RF transceiver of Amos/Guerlin a first phase locked loop as suggested by Applicant's admitted prior art.

One of ordinary skill in this art would have been motivated to include in the RF transceiver a first phase locked loop because they adjust the frequency of the input signal.

Regarding claim 99, Amos/Guerlin disclose the wireless device of claim 98 (see above), wherein the shutdown module shuts down the circuits of the transceiver during said low power mode (Guerlin: col. 2, lines 33-39) and operates the circuits of the transceiver during said active move (Guerlin: col. 2, lines 30-39). Amos/Guerlin fail to disclose wherein said RF transceiver includes a second phase locked loop (PLL).

However, Applicant's admitted prior art discloses wherein said RF transceiver includes a second phase locked loop (PLL) (Background of the Invention: paragraph [0003]; note the plurality of phase locked loops).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include in the RF transceiver of Amos/Guerlin a second phase locked loop as suggested by Applicant's admitted prior art.

One of ordinary skill in this art would have been motivated to include in the RF transceiver a first phase locked loop because they adjust the frequency of the input signal.

Regarding claims 161 and 222, the limitations are rejected for the same reasons and motivations stated above for claim 98.

Regarding claim 162 and 223, the limitations are rejected for the same reasons and motivations stated above for claim 99.

38. Claims 117, 121, 125, 132, 138, 143, 148, 152, 180, 184, 188, 195, 201, 206, 211, 215, 237, 244, 251 and 257 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama in view of Chapman.

Regarding claim 117, Aoyama discloses the wireless device of claim 114. Aoyama fails to disclose wherein said first oscillator includes a crystal oscillator and said second oscillator includes a semiconductor oscillator.

However, Chapman discloses a wireless device with active and low power modes wherein said first oscillator includes a crystal oscillator (col. 4, lines 33-54) and said second oscillator includes a semiconductor oscillator (col. 4, lines 33-54).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the second oscillator of Aoyama to include a semiconductor oscillator as suggested by Chapman.

One of ordinary skill in this art would have been motivated to incorporate the second oscillator to include a semiconductor oscillator because it has the characteristics of drawing very little power in both sleep and stop modes (Chapman: col. 4, lines 39-43).

Regarding claim 121, Aoyama discloses the wireless device of claim 114. Aoyama fails to disclose wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode.

However, Chapman discloses a wireless device with active and low power modes wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode (from col. 2, line 65 through col. 3, line 5).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to calibrate said second reference frequency of said second oscillator using said first reference frequency of said first oscillator of Aoyama before transitioning to said low power mode as suggested by Chapman.

One of ordinary skill in this art would have been motivated to calibrate said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode because it would compensate for the inaccuracy of the semiconductor oscillator due to its dependence upon voltage, process and temperature and it's inherent frequency instability (Chapman: from col. 2, line 65 through col. 3, line 5).

Regarding claim 125, Aoyama discloses the wireless device of claim 123 (see above). Aoyama fails to disclose wherein said first oscillator includes a crystal oscillator and said second oscillator includes a semiconductor oscillator.

However, Chapman discloses a wireless device with active and low power modes wherein said first oscillator includes a crystal oscillator (col. 4, lines 33-54) and said second oscillator includes a semiconductor oscillator (col. 4, lines 33-54).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the second oscillator of Aoyama to include a semiconductor oscillator as suggested by Chapman.

One of ordinary skill in this art would have been motivated to incorporate the second oscillator to include a semiconductor oscillator because it has the characteristics of drawing very little power in both sleep and stop modes (Chapman: col. 4, lines 39-43).

Regarding claim 132, Aoyama discloses the wireless device of claim 123 (see above). Aoyama fails to disclose wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode.

However, Chapman discloses a wireless device with active and low power modes wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode (from col. 2, line 65 through col. 3, line 5).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to calibrate said second reference frequency of said second oscillator using said first reference frequency of said first oscillator of Aoyama before transitioning to said low power mode as suggested by Chapman.

Regarding claim 138, Aoyama discloses the wireless device of claim 137. Aoyama fails to disclose wherein said first oscillator includes a crystal oscillator and said second oscillator includes a semiconductor oscillator.

However, Chapman discloses a wireless device with active and low power modes wherein said first oscillator includes a crystal oscillator (col. 4, lines 33-54) and said second oscillator includes a semiconductor oscillator (col. 4, lines 33-54).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the second oscillator of Aoyama to include a semiconductor oscillator as suggested by Chapman.

One of ordinary skill in this art would have been motivated to incorporate the second oscillator to include a semiconductor oscillator because it has the characteristics of drawing very little power in both sleep and stop modes (Chapman: col. 4, lines 39-43).

Regarding claim 143, Aoyama discloses the wireless device of claim 137. Aoyama fails to disclose wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode.

However, Chapman discloses a wireless device with active and low power modes wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode (from col. 2, line 65 through col. 3, line 5).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to calibrate said second reference frequency of said second oscillator

using said first reference frequency of said first oscillator of Aoyama before transitioning to said low power mode as suggested by Chapman.

One of ordinary skill in this art would have been motivated to calibrate said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode because it would compensate for the inaccuracy of the semiconductor oscillator due to its dependence upon voltage, process and temperature and it's inherent frequency instability (Chapman: from col. 2, line 65 through col. 3, line 5).

Regarding claim 148, Aoyama discloses the wireless device of claim 145. Aoyama fails to disclose wherein said first oscillator includes a crystal oscillator and said second oscillator includes a semiconductor oscillator.

However, Chapman discloses a wireless device with active and low power modes wherein said first oscillator includes a crystal oscillator (col. 4, lines 33-54) and said second oscillator includes a semiconductor oscillator (col. 4, lines 33-54).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the second oscillator of Aoyama to include a semiconductor oscillator as suggested by Chapman.

One of ordinary skill in this art would have been motivated to incorporate the second oscillator to include a semiconductor oscillator because it has the characteristics of drawing very little power in both sleep and stop modes (Chapman: col. 4, lines 39-43).

Regarding claim 152, Aoyama discloses the wireless device of claim 145. Aoyama fails to disclose wherein said shutdown module selectively calibrates said second reference frequency

of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode.

However, Chapman discloses a wireless device with active and low power modes wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode (from col. 2, line 65 through col. 3, line 5).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to calibrate said second reference frequency of said second oscillator using said first reference frequency of said first oscillator of Aoyama before transitioning to said low power mode as suggested by Chapman.

One of ordinary skill in this art would have been motivated to calibrate said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode because it would compensate for the inaccuracy of the semiconductor oscillator due to its dependence upon voltage, process and temperature and it's inherent frequency instability (Chapman: from col. 2, line 65 through col. 3, line 5).

Regarding claim 180, the limitations are rejected for the same reasons and motivations stated above for claim 117.

Regarding claims 184 and 237, the limitations are rejected for the same reasons and motivations stated above for claim 121.

Regarding claim 188, the limitations are rejected for the same reasons and motivations stated above for claim 125.

Regarding claims 195 and 244, the limitations are rejected for the same reasons and motivations stated above for claim 132.

Regarding claim 201, the limitations are rejected for the same reasons and motivations stated above for claim 138.

Regarding claim 206 and 251, the limitations are rejected for the same reasons and motivations stated above for claim 143.

Regarding claim 211, the limitations are rejected for the same reasons and motivations stated above for claim 148.

Regarding claims 215 and 257, the limitations are rejected for the same reasons and motivations stated above for claim 152.

39. Claims 109-110, 118-119, 149-150, 172-173, 181-182, 212-213, 229-230, 235-236, and 255-256 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama/Guerlin and further in view of Applicant's admitted prior art.

Regarding claim 118, Aoyama/Guerlin disclose the wireless device of claim 118 (see above), wherein the shutdown module shuts down the circuits of the transceiver during said low power mode (Guerlin: col. 2, lines 33-39) and operates the circuits of the transceiver during said active move (Guerlin: col. 2, lines 30-39). Aoyama/Guerlin fail to disclose wherein said RF transceiver includes a first phase locked loop (PLL).

However, Applicant's admitted prior art discloses wherein said RF transceiver includes a first phase locked loop (PLL) (Background of the Invention: paragraph [0003]).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include in the RF transceiver of Aoyama/Guerlin a first phase locked loop as suggested by Applicant's admitted prior art.

One of ordinary skill in this art would have been motivated to include in the RF transceiver a first phase locked loop because they adjust the frequency of the input signal.

Regarding claim 119, Aoyama/Guerlin disclose the wireless device of claim 118 (see above), wherein the shutdown module shuts down the circuits of the transceiver during said low power mode (col. 2, lines 33-39) and operates the circuits of the transceiver during said active move (col. 2, lines 30-39). Aoyama/Guerlin fail to disclose wherein said RF transceiver includes a second phase locked loop (PLL).

However, Applicant's admitted prior art discloses wherein said RF transceiver includes a second phase locked loop (PLL) (Background of the Invention: paragraph [0003]; note the plurality of phase locked loops).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include in the RF transceiver of Aoyama/Guerlin a second phase locked loop as suggested by Applicant's admitted prior art.

Regarding claims 109, 149, 172, 181, 212, 229, 235, and 255, the limitations are rejected for the same reasons and motivations stated above for claim 118.

Regarding claims 110, 150, 173, 182, 213, 230, 236, and 256, the limitations are rejected for the same reasons and motivations stated above for claim 119.

40. Claims 129, 140, 192, 203, 242, and 249 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama in views of Guerlin and Applicant's admitted prior art.

Regarding claim 140, Aoyama discloses the wireless device of claim 134 (see above). Aoyama fails to disclose wherein said first wireless circuit includes a first phase locked loop (PLL) and wherein said shutdown module shuts down said first PLL during said low power mode and operates said first PLL during said active mode.

However, Guerlin discloses a wireless device with active and low power modes wherein said first wireless circuit (col. 1, lines 55-63; col. 2, lines 33-39; note the transceiver) includes circuitry and wherein said shut down module shouts down said first circuitry during said low power mode (col. 2, lines 33-39) and operates said circuitry during said active mode (col. 2, lines 33-39).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate in the wireless circuit of Aoyama circuitry wherein said shut down module shouts down said first circuitry during said low power mode (col. 2, lines 33-39) and operates said circuitry during said active mode as suggested by Guerlin.

One of ordinary skill in this art would have been motivated to incorporate in the wireless circuit of Aoyama circuitry wherein said shut down module shouts down said first circuitry during said low power mode and operates said circuitry during said active mode because they are the typical components of a wireless, e.g., a mobile telephone (Guerlin: col. 1, lines 55-63).

Aoyama/Guerlin fails to disclose wherein said first wireless circuit includes a first phase locked loop (PLL).

However, Applicant's admitted prior art discloses wherein said wireless circuit (note the transceiver) includes a first phase locked loop (PLL) (Background of the Invention: paragraph [0003]).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include in the wireless circuit of Aoyama/Guerlin a first phase locked loop as suggested by Applicant's admitted prior art.

Regarding claims 129, 192, 203, 242 and 249, the limitations are rejected for the same reasons and motivations stated above for claim 140.

41. Claims 103-104, 106-107, 111, 166-167, 169-170, 174, and 226-228 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama in view of Guerlin.

Regarding claim 103, Aoyama discloses a wireless device with active and low power modes, comprising; a voltage supply that supplies a first voltage level (Figs. 3 and 9, reference numeral Vdd) and a second voltage level (Figs. 3 and 9, reference numeral 1); and a shutdown module transitions from said first voltage level to said second voltage level when transitioning from said active mode to said low power mode (from col. 7, line 66 through col. 8, line 2), and transitions from said second voltage level to said first voltage level when transitioning from said low power mode to said active mode (col. 7, lines 39-49 and col. 8, lines 28-39).

Aoyama fails to disclose a radio frequency (RF) transceiver that transmits and receives RF signals; a baseband processor (BBP) that communicates with said RF transceiver and that performs RF mixing; and a shutdown module that shuts down said BBP and said RF transceiver in said low power mode and that operates said BBP and said RF transceiver in said active mode.

However, Guerlin discloses a wireless device with active and low power modes comprising: a radio frequency (RF) transceiver that transmits and receives RF signals (Fig. 1, reference numeral 11; col. 1, lines 55-63); a baseband processor (BBP) that communicates with said RF transceiver and that performs RF mixing (col. 1, lines 55-63), and a shutdown module

shuts down said RF transceiver and said BBP during said low power mode (col. 2, lines 33-39) and operates said BBP and said RF transceiver during said active mode (col. 2, lines 30-33).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate in the wireless device of Aoyama a radio frequency (RF) transceiver that transmits and receives RF signals, a baseband processor (BBP) that communicates said RF transceiver and that performs RF mixing, wherein said shutdown module shuts down said RF transceiver and said BBP during said low power mode and operates said BBP and said RF transceiver during said active mode as suggested by Guerlin.

One of ordinary skill in this art would have been motivated to incorporate in the wireless device a radio frequency (RF) transceiver that transmits and receives RF signals; and a baseband processor (BBP) that communicates with said RF transceiver and that performs RF mixing because they are all typical components in a wireless device, e.g., a mobile phone (Guerlin: col. 1, lines 55-63), wherein said shutdown module shuts down said RF transceiver and said BBP during said low power mode and operates said BBP and said RF transceiver during said active mode for maximum energy conservation (Guerlin: col. 2, lines 33-39).

Regarding claim 104, in the obvious combination, Aoyama discloses wherein said voltage supply includes a first voltage supply that supplies said first voltage level (Figs. 3 and 9, reference numeral Vdd) and a second voltage supply that supplies said second voltage level (Figs. 3 and 9, reference numeral 1).

Regarding claim 106, in the obvious combination, Aoyama discloses further comprising a first oscillator that communicates with said BBP and said RF transceiver (Figs. 3 and 9, reference numeral 3; note that in the obvious combination of Aoyama/Guerlin, the first oscillator

of Aoyama will communicate with the BBP and RF transceiver of Guerlin), that receives said first voltage level and that generates a first reference frequency (Figs. 3 and 9).

Regarding claim 107, in the obvious combination, Aoyama discloses further comprising a second oscillator that receives said second voltage level, that consumes less power than said first oscillator and that generates a second reference frequency (Figs. 3 and 9, reference numeral 4; col. 5, lines 9-11).

Regarding claim 111, in the obvious combination, Aoyama discloses wherein said first voltage supply includes a first voltage regulator (Figs. 3 and 9, reference numeral Vdd) and said second voltage supply includes a second voltage regulator (Figs. 3 and 9, reference numeral 1).

Regarding claims 166 and 226, the limitations are rejected for the same reasons and motivations stated above for claim 103.

Regarding claim 167, the limitations are rejected for the same reasons and motivations stated above for claim 104.

Regarding claims 169 and 227, the limitations are rejected for the same reasons and motivations stated above for claim 106.

Regarding claims 170 and 228, the limitations are rejected for the same reasons and motivations stated above for claim 107.

Regarding claim 174, the limitations are rejected for the same reasons and motivations stated above for claim 111.

42. Claims 105, 113, 176, 168, and 232 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama/Guerlin as applied to claim 103 above and further in view of Amos.

Regarding claim 105, Aoyama/Guerlin discloses the wireless device of claim 103 (see above). Aoyama/Guerlin fails to disclose further comprising a medium access controller (MAC) device that includes said shutdown module.

However, Amos discloses a wireless device with active and low power modes further comprising a medium access controller (MAC) device that includes said shutdown module (from col. 2, line 61 through col. 3, line 8).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to include the shutdown module of Aoyama/Guerlin in a medium access controller (MAC) device as suggested by Amos.

One of ordinary skill in this art would have been motivated to include the shutdown module in a medium access controller (MAC) device because it is required to be responsive to the host bus interface and events from a wireless or RF interface (Amos: col. 1, lines 41-43).

Regarding claim 168, the limitations are rejected for the same reasons and motivations stated above for claim 105.

Regarding claim 113, Aoyama/Guerlin discloses a system comprising the wireless device of claim 103 (see above). Aoyama/Guerlin fails to disclose further comprising a remote device for periodically transmitting a beacon, wherein said shutdown module transitions said wireless device from said low power mode prior to receiving a beacon.

However, Amos discloses a system comprising a wireless device with active and low power modes further comprising a remote device for periodically transmitting a beacon, wherein said shutdown module transitions said wireless device from said low power mode prior to receiving a beacon (col. 1, lines 62-65; col. 5, lines 1-8).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to further comprise in the system of Aoyama/Guerlin remote device for periodically transmitting a beacon, wherein said shutdown module transitions said wireless device from said low power mode prior to receiving a beacon as suggested by Amos.

One of ordinary skill in this art would have been motivated to further comprise in the system remote device for periodically transmitting a beacon, wherein said shutdown module transitions said wireless device from said low power mode prior to receiving a beacon because the system would determine if there is any activity that needs to be handled (Amos: col. 5, lines 8-9).

Regarding claims 176 and 232, the limitations are rejected for the same reasons and motivations stated above for claim 113.

43. Claims 108, 112, 171, 175, and 231 are rejected under 35 U.S.C. 103(a) as being unpatentable over Aoyama/Guerlin in view of Chapman.

Regarding claim 108, Aoyama/Guerlin discloses the wireless device of claim 107. Aoyama/Guerlin fails to disclose wherein said first oscillator includes a crystal oscillator and said second oscillator includes a semiconductor oscillator.

However, Chapman discloses a wireless device with active and low power modes wherein said first oscillator includes a crystal oscillator (col. 4, lines 33-54) and said second oscillator includes a semiconductor oscillator (col. 4, lines 33-54).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to incorporate the first oscillator of Aoyama/Guerlin to include a crystal

oscillator as suggested by Chapman and to incorporate the second oscillator of Aoyama/Guerlin to include a semiconductor oscillator as suggested by Chapman.

One of ordinary skill in this art would have been motivated to incorporate the first and second oscillators to include a crystal oscillator and semiconductor oscillator, respectively because it has the characteristics of drawing very little power in both sleep and stop modes (Chapman: col. 4, lines 39-43).

Regarding claim 112, Aoyama/Guerlin discloses the wireless device of claim 107. Aoyama/Guerlin fails to disclose wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode.

However, Chapman discloses a wireless device with active and low power modes wherein said shutdown module selectively calibrates said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode (from col. 2, line 65 through col. 3, line 5).

Therefore, it would have been obvious to one of ordinary skill in this art at the time of invention by applicant to calibrate said second reference frequency of said second oscillator using said first reference frequency of said first oscillator of Aoyama/Guerlin before transitioning to said low power mode as suggested by Chapman.

One of ordinary skill in this art would have been motivated to calibrate said second reference frequency of said second oscillator using said first reference frequency of said first oscillator before transitioning to said low power mode because it would compensate for the inaccuracy of the semiconductor oscillator due to its dependence upon voltage, process and

temperature and it's inherent frequency instability (Chapman: from col. 2, line 65 through col. 3, line 5).

Regarding claims 171, the limitations are rejected for the same reasons and motivations stated above for claim 108.

Regarding claims 175 and 231, the limitations are rejected for the same reasons and motivations stated above for claim 112.

Allowable Subject Matter

44. Claim 18, 48, and 78 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

45. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Marivelisse Santiago-Cordero whose telephone number is (571) 272-7839. The examiner can normally be reached on Monday through Friday from 7:30am to 4:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lester Kincaid can be reached on (571) 272-7922. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

10/3/05

LESTER G. KINCAID
SUPERVISORY PRIMARY EXAMINER